SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation-in-Part of Application No. _________, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al. (Attorney docket No. 1875.2830000); and is related to Application No. _________, Filed: May 31, 2002; Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER et al. (Attorney docket No. 1875.2810000); Application No. _________, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER (Attorney docket No. 1875.2790000); and Application No. _________, Filed: May 31, 2002, Inventor: Jan MULDER; Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, Inventors: Jan MULDER et al. (Attorney docket No. 1875.2800000), all of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to analog to digital converters ADC, and more particularly, to analog to digital converters utilizing track-and-hold amplifiers for high speed operation.

Related Art

[0003] A subranging analog to digital converter (ADC) architecture is suitable for implementing high-performance ADC's (i.e. high speed, low power, low area, high resolution). FIG. 1 shows the generic two-step subranging architecture, comprising a reference ladder 104, a coarse ADC 102, a switching matrix 103, a fine ADC 105, coarse comparators (latches) 107, fine comparators (latches) 108 and an encoder 106. In most cases, a track-and-hold 101 is used in front of the ADC. In this architecture, an input voltage is first quantized by the coarse ADC 102. The coarse ADC 102 and the coarse comparators 107 compare the input voltage against all the reference voltages, or against a subset of the reference voltages that is uniformly distributed across the whole range of reference voltages. Based on a coarse quantization, the switching matrix 103 connects the fine ADC 105 and the fine comparators 108 to a subset of the reference voltages (called a "subrange") that is centered around the input signal voltage. The coarse and fine comparators 107, 108 latch the outputs of the coarse and fine ADC's 102, 105 prior to inputting them to the encoder 106.

[0004] High-speed high-resolution ADC's usually use a track-and-hold (T/H) or a sample-and-hold (S/H) preceding the ADC. The main distinction between a S/H and a T/H is that a S/H holds the sampled input signal for (almost) a full clock period, whereas a T/H holds the sampled input signal for (almost) half a clock period.

[0005] In general, a S/H requires more area and power than a T/H to obtain the same performance. However, the disadvantage of a T/H is that the sampled input signal is available to the ADC for only half a clock period.

[0006] Other subranging ADC's are known that can use a T/H instead of a S/H. However, the timing proposed in conventional art has important disadvantages.

[0007] Typically, both the coarse and fine ADC amplifiers reset to the T/H output voltage. This leaves much less time available for the coarse ADC amplifiers to

amplify the signals and the coarse comparators to decide on a voltage to latch. This will impact a maximum sampling speed F_{sample} that the ADC can run at.

[0008] Some ADC's use a T/H, where the same physical circuits are used for performing both the coarse and the fine quantization. This leaves only 1/4 of a clock cycle available for performing the coarse quantization, or two time-interleaved sub-ADC's have to be used. This impacts either maximum possible operating speed, or doubles required area and power.

[0009] Thus, one of the bottlenecks in subranging ADC's is the limited amount of time available for performing the coarse quantization. Several different timing methods for subranging ADC's are known for optimizing this bottleneck. Unfortunately, most of these solutions require the use of a S/H, or use time-interleaved ADC's. This disadvantageously affects the required power and area.

SUMMARY OF THE INVENTION

[0010] The present invention is directed to an analog to digital converter that substantially obviates one or more of the problems and disadvantages of the related art.

[0011] There is provided an N-bit analog to digital converter including a reference ladder, a track-and-hold amplifier connected to an input voltage, and a coarse ADC amplifier connected to a coarse capacitor at its input and having a coarse ADC reset switch controlled by a first clock phase of a two-phase clock. A fine ADC amplifier connected to a fine capacitor at its input and has a fine ADC reset switch controlled by a second clock phase of the two-phase clock. A switch matrix selects a voltage subrange from the reference ladder for use by the fine ADC amplifier based on an output of the coarse ADC amplifier. The coarse capacitor is charged to a coarse reference ladder voltage during the first clock phase and connected to the T/H output voltage during the second clock phase, wherein the fine capacitor is connected to a voltage subrange during the first clock phase and to the T/H output voltage during the second clock phase. An

encoder converts outputs of the coarse and fine ADC amplifiers to an N-bit output.

[0012] In another aspect of the present invention there is provided an N-bit analog to digital converter including a reference ladder, a track-and-hold amplifier tracking an input voltage, a two-phase clock having phases φ_1 and φ_2, and a plurality of coarse ADC amplifiers each connected to a corresponding coarse capacitor at its input. The coarse ADC amplifiers are reset on φ_1 and their corresponding coarse capacitors are connected to the T/H output voltage on φ_2. A plurality of fine ADC amplifiers are each connected to a corresponding fine capacitor at their input. The fine ADC amplifiers are reset on φ_2 and their corresponding fine capacitors are charged to the T/H output voltage on φ_2. A switch matrix selects a voltage subrange from the reference ladder based on outputs of the coarse ADC amplifiers for input to the fine ADC amplifiers on φ_1. An encoder converts outputs of the coarse and fine ADC amplifiers to an N-bit output.

[0013] In another aspect of the present invention there is provided a N-bit analog to digital converter including a reference ladder, a track-and-hold amplifier tracking an input voltage, a two-phase clock having phases φ_1 and φ_2, a coarse capacitor connected to the track-and-hold amplifier on φ_2 and to the reference ladder on φ_1, a coarse ADC amplifier that resets on φ_1 and amplifies a voltage on the coarse capacitor on φ_2, and a coarse comparator for latching an output of the coarse ADC amplifier on $\varphi_{1+1\,cycle}$. A fine capacitor is connected to the track-and-hold on φ_2 and to a fine voltage tap of the reference ladder on φ_1, the fine voltage tap selected based on the output of the coarse ADC amplifier. A fine ADC amplifier includes a plurality of cascaded amplifier stages. A first cascaded amplifier stage resets on φ_2 and amplifies a voltage on the fine capacitor on $\varphi_{1+1cycle}$, a second cascaded amplifier stage resets on $\varphi_{1+1cycle}$ and amplifies the voltage on the fine capacitor on $\varphi_{2+1\,cycle}$, a third cascaded amplifier stage resets on $\varphi_{2+1cycle}$ and amplifies the voltage on the fine capacitor on $\varphi_{1+2\,cycles}$, and so on. A fine comparator latches an output of a last cascaded amplifier stage on $\varphi_{1+3\,cycles}$,

and an encoder converts outputs of the coarse and fine comparators to an N-bit output.

[0014] In another aspect of the present invention there is provided an N-bit analog to digital converter including a reference ladder, a track-and-hold amplifier tracking an input voltage, a two-phase clock having alternating phases φ_1 and φ_2, a plurality of coarse capacitors connected to an output of the track-and-hold on φ_2 and to corresponding coarse taps of the reference ladder on φ_1, and a plurality of coarse ADC amplifiers that reset on φ_1 and amplify voltages on the coarse capacitors on φ_2. A plurality of coarse comparators latches outputs of the coarse ADC amplifiers. A plurality of fine capacitors connected to the output of track-and-hold amplifier on φ_2 and connected to fine voltage taps of the reference ladder on φ_1, the fine voltage taps are selected based on the outputs of the coarse ADC amplifiers. A plurality of fine ADC amplifiers, each including a plurality of cascaded amplifier stages. The cascaded amplifier stages reset and amplify on alternating phases φ_1 and φ_2, wherein amplifiers of the first stage are reset on φ_2 and amplify voltages of the fine capacitors on φ_1, a plurality of fine comparators for latching outputs of a last amplifier stage. An encoder converts outputs of the coarse and fine comparators to an N-bit output.

[0015] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0018] FIG. 1 illustrates a conventional subranging ADC architecture;

[0019] FIG. 2 illustrates connections of one set of amplifiers of the present invention;

[0020] FIG. 3 illustrates a timing diagram for operation of the circuit of FIG. 2;

[0021] FIG. 4 shows a pipelined timing diagram for the present invention;

[0022] FIG. 5 shows the timing diagram of the present invention in additional detail; and

[0023] FIGs. 6 and 7 show a flow chart for the timing diagram of FIG. 5; and

[0024] FIGs. 8 and 9 show the coarse and fine ADC's as amplifier arrays.

DETAILED DESCRIPTION OF THE INVENTION

[0025] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0026] This disclosure describes a subranging ADC that uses a two-phase clock timing method that permits the use of a T/H instead of a S/H, thus enabling a low-power, low-area implementation on a chip. The timing technique described herein can use a T/H, instead of a S/H, and does not require time-interleaved ADC's in order to realize high-speed operation.

[0027] FIG. 2 shows a single coarse amplifier A_C and a single fine amplifier A_F that illustrate the proposed timing method of the present invention. Preferably, the coarse amplifier A_C and the fine amplifier A_F are implemented using auto-zero amplifiers. See, e.g., http://www.web-ee.com/primers/files/auto-zero_amps.pdf, for a general discussion of auto-zero amplifiers. (To the extent the overall block

diagram of the architecture is the same as that in FIG. 1, the same reference labels will be used herein. It is also understood that the coarse ADC 102 and the fine ADC 105 actually include an array of coarse amplifiers and an array of fine amplifiers. See, e.g., The Circuits and Filters Handbook, Wai-Kai Chen, ed., 1995, at 2099, for a discussion of subranging ADC's. See also FIGs. 8 and 9, and discussion below.

[0028] In one embodiment, 30 coarse amplifiers, 30 coarse comparators, 19 fine amplifiers and 65 fine comparators are used.) The coarse amplifier A_C is connected to a capacitor C_1, which in turn is connected to either the output of a track-and-hold 101, or to V_{coarse} from the reference ladder 104. A two-phase clock, including phases φ_1 and φ_2, is used to control switches S_1, S_2 and S_3 of the coarse amplifier A_C. When the phase φ_1 is on, the switches S_2 and S_3 are closed, the switch S_1 is open. With the switch S_3 closed, the coarse ADC amplifier A_C is in a reset mode, and the capacitor C_1 is connected to the reference ladder tap V_{coarse}. Also on φ_1, the switch S_5 is closed, the switches S_4 and S_6 are open, and the fine capacitor C_2 is connected to an appropriate tap of the reference ladder V_{fine}. Note that all of the switches as S_1-S_6 are typically field effect transistor (FET) switches. The switch S_3 may be referred to as a coarse ADC reset switch, and the switch S_6 may be referred to as a fine ADC reset switch. When the phase φ_1 of the two-phase clock is on, the switches S_3 and S_2 are closed, the amplifier A_C is in a reset mode, and the left side of the capacitor C_1 is connected to a tap of the reference ladder (i.e., V_{coarse}). The switch S_1 is open when φ_1 is on.

[0029] On the opposite phase of the two-phase clock (φ_2), when φ_2 is high, the switch S_1 is closed, the switches S_2 and S_3 are open. The switches S_4 and S_6 are closed, and the fine amplifier A_F is in reset mode. Therefore the capacitor C_1 is connected to the track-and-hold output, and the amplifier A_C is in an amplify mode when the clock phase φ_2 is on.

[0030] Thus, the operation of the fine ADC amplifier A_F may be thought of as an inverse of the operation of the amplifier A_C. In other words, when the clock phase φ_2 is on, the left side of the capacitor C_2 is connected to the track-and-hold

through switch S_4, and the amplifier A_F is in the reset mode, since the switch S_6 is closed, and the switch S_5 is open. When the clock phase φ_1 is on, a switch S_5 is closed to connect the capacitor C_2 to V_{fine}, (a subrange from the reference ladder 104), the switches S_4 and S_6 are open, and the amplifier A_F is in the amplify mode. The capacitors C_1 and C_2 are typically 50 to 200 femtofarads.

[0031] During the clock phase φ_1, the coarse amplifiers A_C are reset to the reference ladder 104, while the fine amplifiers A_F amplify the previous sample. During the clock phase φ_2, the coarse amplifiers A_C amplify the next sample, while the fine amplifiers A_F reset to the next sample.

[0032] Thus, there is no need to use a sample and hold amplifier, which uses one clock period for the operation of the coarse ADC 102, and one clock period for the operation of the fine ADC 105. With the arrangement shown in FIG. 2, the fine ADC amplifier A_F has a half cycle latency compared to the coarse ADC amplifier A_C. Thus, one half of a clock cycle is available to do coarse quantization (and ½ cycle is available for fine quantization). During the reset phase, the auto-zero amplifiers can be connected either to the T/H or to a reference voltage. An important difference between these two possibilities is that resetting all amplifiers to a reference voltage requires half a clock cycle less latency in comparison with resetting to the T/H output voltage.

[0033] Therefore, if the coarse ADC amplifiers A_C are reset to a tap of the reference ladder 104, and the fine ADC amplifiers A_F are reset to the T/H 101, half a clock cycle now becomes available for performing the coarse quantization. (See also flowcharts in FIG. 6 and FIG. 7) Because a S/H is not needed with this timing approach, the resulting ADC can be more area- and power-efficient.

[0034] The coarse ADC amplifier A_C has one half of a clock cycle to set switches in the switch matrix 103, in order for the switch matrix 103 to pass the correct V_{fine} reference ladder 104 output to the fine ADC 105. While the amplifiers A_C and A_F require two phases to operate, the capacitors C_1 and C_2 subtract the V_{coarse} from the track-and-hold output, or V_{fine} from the track-and-hold output, respectively.

[0035] Phrased another way, there are two steps involved in the process:

[0036] 1) Charge C_1, while the amplifier A_C is in a reset mode, and the amplifier A_C is providing a low impedance so that C_1 can be charged.

[0037] 2) Release the reset, tie the capacitor C_1 to the amplifier A_C in order for it to amplify the track-and-hold output.

[0038] Thus, the track-and-hold 101 only outputs the signal for half a period, and C_1 is charged early, before the track-and-hold 101 is ready. When the track-and-hold 101 is ready, the amplifier A_C immediately does the amplification.

[0039] Although FIG. 2 shows only one coarse amplifier and one fine ADC amplifier A_F, each can be part of an array of amplifiers in one embodiment of the invention. The amplifiers connect to the T/H during one half clock cycle, and to reference voltage taps (V_{coarse} or V_{fine}) from the reference ladder 104 during a second half clock cycle.

[0040] The amplifiers A_C and A_F are typically differential pair auto-zero amplifiers, with resistive load, preferably done in CMOS technology, e.g., NMOS or PMOS. Alternatively, the amplifiers A_C and A_F can be fabricated using bipolar technology.

[0041] FIG. 3 shows how a two-phase non-overlapping clock can be converted to a three phase clock to better fine tune the ability of the coarse and fine amplifiers A_C, A_F and the comparators 107, 108 settle to their final values. As shown in FIG. 3 (and the flowcharts of FIG. 6 and 7), the phase φ_2 can be split up into φ_2 and φ_{2e}, where φ_{2e} represents an early falling edge of the clock phase φ_2. Similarly, φ_1 can be used to generate a phase φ_{1d_fine}, a delayed φ_1 phase of the clock used by the fine ADC 105. As illustrated by the notations at the top and bottom of FIG. 3, the coarse ADC amplifier A_C starts amplifying on the rising edge of φ_{2e}, and stops amplifying on the falling edge of φ_{2e}. The fine ADC amplifier A_F is in a reset mode during that phase.

[0042] During the next phase of the clock, the coarse amplifier A_C begins resetting on the rising edge of φ_1, and stops resetting on the falling edge of φ_1. The comparators 107 of the coarse ADC 102 have from between the falling edge

of φ_{2e} through the rising edge of φ_{1d_fine} to decide on whether they are latching 1 or 0 by comparing to a reference voltage from the reference ladder 104. (Each fine amplifier A_F is actually a cascade of amplifiers, GA, GB, GC, GD, as discussed below, and which is particularly useful in a pipelined architecture. The first amplifier in the cascade, GA, amplifies between the rising edge of φ_{1d_fine} through the falling edge of φ_{1d_fine}.)

[0043] FIG. 4 further illustrates the operation of the amplifiers of the present invention in a situation where the fine ADC 105 has 4 cascaded stages (typically with a gain of 4x each), which are labeled GA, GB, GC and GD. In FIG. 4, the amplifier stage of the coarse ADC 102 is labeled GE, the coarse ADC comparator 107 is labeled CC, the fine ADC comparator 108 is labeled FC and the encoder is labeled ENC. The gray portions of FIG. 4 illustrate a progression of one sample's quantization down the amplifier cascade. First, the track-and-hold 101 is connected to the coarse ADC amplifier A_C, during phase φ_2. Meanwhile, the coarse comparator 107 (CC) is reset during φ_2. The fine ADC amplifier A_F stage GA is also reset. During the next phase φ_1, the first stage GA of the fine ADC 105 amplifies, while the second stage GB resets. The process continues, as the signal moves in a pipelined manner down from GA to GB to GC to GD to the fine comparator 108 (FC), and ultimately to the encoder 106. The next quantization is directly behind the quantization just performed, moving from left to right in the figure, and offset by one clock cycle from the measurement illustrated in gray in FIG. 4.

[0044] FIGs. 5 and 6 illustrates the operation of the coarse/fine ADC's 102/105 in greater detail, showing the relationship between the clock phases of the three phase clock discussed above, and the operation of the various components shown in FIG. 2. As may be seen from FIGs. 5 and 6, the coarse capacitor C_1 is connected to the reference ladder 104 voltage V_{ref} (i.e., V_{coarse}) on the rising edge of the clock phase φ_1. The coarse amplifier 102 is also reset on the rising edge of φ_1, with the switch S_3 being closed until the falling edge of φ_1. The switch S_2 is kept closed until the falling edge of φ_{1d} (the delayed edge of φ_1).

[0045] On the rising edge of φ_2, the coarse capacitor C_1 is connected to the track-and-hold 101, and the coarse amplifier A_C begins amplifying the signal. The coarse comparator 107 (CC) is reset on the rising edge of φ_2, and the fine capacitor C_2 is connected to the track-and-hold voltage. The fine amplifier A_F is also reset on the rising edge of φ_2. The coarse capacitor C_1 is connected to the track-and-hold 101 until the falling edge of φ_{2d} (for delayed φ_2), the coarse comparator 107 (CC) begins latching at the falling edge of φ_{2e} (for early φ_2) and the fine amplifier A_F continues to be reset until the falling edge of φ_2. The fine capacitor C_2 is connected to the T/H through the delayed falling edge of φ_2 (φ_{2d}).

[0046] On the next half clock cycle φ_1, the coarse comparator 107 (CC) is assumed to have latched at the rising edge of φ_{1d_fine}, while the fine capacitor C_2 is connected to the reference voltage and fine amplifier A_F begins to amplify, also on the rising edge of φ_{1d_fine}. The connection of the capacitor C_2 to the reference ladder 104 lasts until the falling edge of φ_{1d}, and the fine amplifier A_F stops amplifying on the falling edge of φ_{1d}.

[0047] The digital output of the coarse ADC tells the fine ADC 105 which subrange from the reference ladder voltage V_{ref} (i.e., V_{fine}) the switch matrix 103 should pass through to the fine ADC 105. Each amplifier amplifies only if there is a valid signal period. Here, the hold phase is the middle 1/3 phase of FIG. 5 - both the coarse amplifier A_C and the fine amplifier A_F are looking at the signal. In a particular embodiment, an array of 30 coarse amplifiers and an array of 30 coarse comparators are used to get 31 subranges. The switch matrix 103 therefore connects to one out of 31 subranges. On the fine amplifier A_F side, the embodiment includes an array of 19 A-stage amplifiers, an array of 33 B-stage amplifiers, an array of 65 C-stage amplifiers and an array of 65 D-stage amplifiers, as well as an array of 65 fine comparators. The coarse ADC 102 of the present invention is illustrated in array form in FIG. 8, showing a plurality of amplifiers A_{C0} - A_{Cm}, connected to a plurality of input capacitors C_{C0}, and through the input capacitors C_{Cm} to a plurality of coarse taps from the reference ladder 104, taps $V_{coarse,0}$ to $V_{coarse,m}$. For 30 coarse amplifiers, m=29.

[0048] Similarly, the fine ADC 105 of the present invention is illustrated in array form in FIG. 9, showing a plurality of amplifiers A_{F0} - $A_{Fn,}$ connected to a plurality of input capacitors C_{F0}, and through the input capacitors C_{Fn} to a plurality of fine taps from the reference ladder 104, taps $V_{fine,0}$ to $V_{fine,n}$. For 19 fine amplifiers, n=18. Note that although the auto-zero amplifiers A_{C0} - A_{Cm} and A_{F0} - A_{Fn} are shown as single ended in FIGs. 8 and 9, in actual application they are preferably differential amplifiers.

[0049] An "11 bit" output is actually converted to a 10-bit output, to compensate for conversion errors of the coarse ADC. With the approach of the present invention, there is no need to have to interleave ADC's running at ½ F_{sample}. Here, a single ADC can be run at F_{sample}, since there is delay of the latency of the fine ADC 105 by one half of a clock cycle.

[0050] Some timing refinements may be incorporated. The switches S_1, S_2 and S_4 shown on the left-side of the sampling capacitors C_1, C_2 in FIG. 2 can use slightly delayed clocks φ_{1d} and φ_{2d}.

[0051] Furthermore, the coarse comparators 107 (CC) use an earlier clock signal φ_{1e}, to give them somewhat more time to compare their input signal, thus improving their bit-error-rate. The switch S_5 connecting the fine amplifiers A_F to the reference ladder 104 use a delayed clock, φ_{1dfine}, for the same reason. Basically, this implements a three-phase clock to operate the coarse ADC 102.

[0052] The proposed timing can be applied to all subranging ADC's to improve the required power and area.

[0053] It will be appreciated that the various aspects of the invention as further disclosed in related Application No. _________, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al.; Application No. _________, Filed: May 31, 2002; Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, Inventors: Jan MULDER et al.; Application No. _________, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; and Application No. _________, Filed: May 31, 2002, Inventor:

Jan MULDER; Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventor: Jan MULDER, all of which are incorporated by reference herein, may be combined in various ways, or be integrated into a single integrated circuit or product.

[0054] It will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined in the appended claims. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.